WHAT IS CLAIMED IS

1. A high-speed data buffer, comprising:

a rising-edge device having a trigger circuit and a sampling clock generation circuit ; and

a falling-edge device having a trigger circuit and a sampling clock generation circuit;

wherein said buffer extends a timing margin thereof for sampling correct data.

2. The high-speed data buffer as recited in claim 1, wherein said trigger circuit of said rising-edge device comprises a ring counter for receiving a clock signal and counting in response to said clock signal so as to generate a first rising flag signal FLAG R1 and a second rising flag signal FLAG R2.

3. The high-speed data buffer as recited in claim 2, wherein each rising-edge circuit of said rising-edge device comprises a plurality of flip-flops serially connected to store sampled data, wherein said plurality of flip-flops receive a first rising sampling clock signal CLK R1 generated by an AND operation, provided by a first AND gate , of said clock signal and said first rising flag signal FLAG R1 and a second rising sampling clock signal CLK R2 generated by an AND operation, provided by a second AND gate, of said clock signal and said second rising flag signal FLAG R2.

4. The high-speed data buffer as recited in claim 1, wherein said trigger circuit of said falling-edge device comprises a ring counter receiving a clock signal and counting in response to said clock signal, so as to generate a first falling flag signal FLAG F1 and a second falling flag signal FLAG F2.

5. The high-speed data buffer as recited in claim 4, wherein each falling-edge circuit of said falling-edge device comprises a plurality of flip-flops serially connected to store sampled data, wherein said plurality of

flip-flops receive a first falling sampling clock signal CLK F1 generated by an OR operation, provided by a first OR gate, of said clock signal and said first falling flag signal FLAG F1 and a second falling sampling clock signal CLK F2 generated by an OR operation, provided by a second OR gate, of said clock signal and said second falling flag signal FLAG F2.

6. The high-speed data buffer as recited in claim 2, wherein said ring counter comprises a plurality of D-type flip-flops.

7. The high-speed data buffer as recited in claim 4, wherein said ring counter comprises a plurality of D-type flip-flops.

8. The high-speed data buffer as recited in claim 3, wherein said flip-flops of said rising-edge circuit are D-type flip-flops.

9. The high-speed data buffer as recited in claim 5 wherein said flip-flops of said falling-edge circuit are D-type flip-flops.

10.The high-speed data buffer as recited in claim 2, further comprising a D-type flip-flop to provide said ring counter with said clock signal.

11.A high-speed data buffer, comprising:

a rising-edge device and a falling-edge device, wherein said rising-edge device comprises:

a ring counter, operative for generating a rising flag signal for data sampling; and

a rising-edge circuit, comprising a plurality of flip-flops serially connected, wherein said plurality of flip-flops are clocked by an AND operation output, provided by an AND gate, of said clock signal and said rising flag signal;

said falling-edge device comprises:

a ring counter, operative for generating a falling flag signal for data sampling; and

a falling-edge circuit, comprising a plurality of flip-flops serially

connected, wherein said plurality of flip-flops are clocked by an OR operation output, provided by an OR gate, of said clock signal and said falling flag signal.

12. The high-speed data buffer as recited in claim 11, wherein said ring counters comprise a plurality of D-type flip-flops.

13. The high-speed data buffer as recited in claim 11, wherein said flip-flops are D-type flip-flops.

14. A high-speed data buffer, comprising:

a ring counter, operative for generating a falling flag signal for data sampling; and

a falling-edge circuit, clocked by an OR operation output, provided by an OR gate, of said clock signal and said falling flag signal;

wherein , while an excess pulse edge occurs when the data transfer is performed in a low-level region, data sampled by the excess pulse edge is incorrect ,said falling-edge circuit is capable of overwriting said incorrect sampled data with subsequent correct data so as to ensure sampling correct data.

15. The high-speed data buffer as recited in claim 14, wherein said ring counter comprises a plurality of D-type flip-flops.

16. The high-speed data buffer as recited in claim 14, wherein said plurality of falling-edge circuits comprises a plurality of D-type flip-flops serially connected.

17. The high-speed data buffer as recited in claim 14, wherein said falling-edge circuit comprises a plurality of flip-flops serially connected.